Bodepu Sai Tirumala Naidu

Edge AI Engineer · FPGA Design

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Education

Indian Institute of Information Technology, Design and Manufacturing *Jabalpur, India*

Bachelor of Technology in Electronics and Communication Engineering *Aug. 2017 -May. 2021*

- **Thesis**: Implementation of Deep Learning Accelerator with RISC-V SoC on FPGA

Skills

Hardware Languages	Verilog, System Verilog
Software Languages	C/C++, Python, Bash
FPGA and ASIC Tools	Xilinx Vivado, Intel Quartus Prime, Synopsys DC, QuestaSim
Others	Good Knowledge of AI inference runtime pipelines, neural network quantization & pruning for edge and deployment of edge devices. Basic knowledge of low-level software such as drivers and firmware. Usage of scrum agile methodology in projects and collaboration using tools such Git, Jira, etc.

Work Experience

SandLogic Technologies *Bangalore, India*

Edge AI Engineer (Deep Learning Accelerator Design) *Jul. 2021 - Present*

Involved in RTL Design, FPGA Implementation and writing test applications in C++ for the in-house deep learning accelerator. Tasks included but were not limited to:

- Pipelining the hardware to achieve timing closure and good knowledge on various Ultrafast design methodology techniques to achieve the optimum PPA on the FPGA.
- Experience on optimizing FPGA resource utilization by analyzing the RTL logic and instantiating the suitable FPGA hardware primitives such as DSP48, URAM, BRAM etc.
- Performed system performance benchmarking and bandwidth bottleneck analysis on ZU+ MPSoC and in-house AI accelerator using Vivado and Vitis tools and IPs such as AXI performance monitors.
- Experience with various In-system Logic Design Debugging flows using IPs such as System ILA and VIO.
- RTL Design of DMA module which acts as a bridge between the DRAM and SRAM for the accelerator.
- Implementation of AMBA AXI4 bus interface in verilog.
- Generation of Petalinux image and kernel configuration for the exported hardware FPGA platform.

SandLogic Technologies *Bangalore, India*

Hardware Intern *Oct. 2020 - Jul. 2021*

- Worked as part of the AI hardware team to integrate Deep Learning Accelerators to ARM and RISC-V SoCs on Zynq Ultrascale+ Platform and Artix-7 FPGAs.
- Integrated a Multi-Port Memory Controller (MPMC) design to share the DDR Memory Controller between SoC and Accelerator.
- Gained adequate knowledge of AXI Protocol and various AXI Infrastructure Architectures.
- Optimizing the FPGA design using various inbuilt Vivado strategies, timing analysis and placement & routing.
- Porting the Kernel drivers and Runtime of Accelerator to the RISC-V Linux kernel and successfully running various DL models.

Independent Research Group *Remote*

Part time Researcher *Dec. 2020 - Present*

Research Guides: Dr. Arnab Raha, Staff Research Scientist, Intel and Dr. Amitava Mukherjee, Professor, School of Computing, Amrita

Topic: Working on various research areas in designing ASIC based Edge AI platforms for various biomedical applications such as MR imaging and ECG.

Publications

SCENIC: An Area and Energy-Efficient CNN-based Hardware Accelerator for Discernable Classification of Brain Pathologies using MRI

VLSID 2022: 35th International Conference of VLSI Design and the 21st International Conference on Embedded Systems, India

Academic Projects

OpenCL based Neural Network Accelerator on FPGA for image classification

Oct. 2019 - Jun. 2020

Mentor: Dr. Vinod Kumar Jain, Assistant Professor, IIIT Jabalpur

- Designed a DNN Accelerator for Darknet Reference Model (which is 3 times faster then Alexnet and attains the same accuracy as Alexnet) on Intel Cyclone V SoC FPGA using High Level Synthesis (HLS) toolchain.
- OpenCL-CNN-Accelerator when integrared to ARM Cortex A9 processor achieved around 300% faster inference throughput than CPU alone.

Pulse Oximeter system using Fast Fourier Transform (FFT)

Oct. 2018 - May 2019

Mentor: Dr. Varun Bajaj, Associate Professor, IIIT Jabalpur

- Usually in Pulse oximeters, we calculate blood oxygen level (SpO2) using time series analysis of PPG signal we obtain from the oximeter sensors.
- In this project, we measured the blood oxygen level through spectral analysis of PPG data of a patient using Fast Fourier Transform in MatLab. This method may be helpful in low power, low cost, portable oximetry applications.

IoT based Power Management System for frequency based electricity pricing

Oct. 2018 - May 2019

Mentor: Dr. Sachin Kumar Jain, Assistant Professor, IIIT Jabalpur

- Developed an automated power management system which considers Availability Based Tariff (ABT) or frequency-based pricing mechanism nd optimizes appliances use to get the lowest power bill.
- pricing mechanism helps to maintain constant frequency across the entire power grid. Presently ABT mechanism is used just to bill the power usage of large scale industries but there is a possibility to use for household power grid.

Honors & Awards

Finalist, Swadeshi Microprocessor Challenge, MeitY, GoI

2021

Top-30 Amongst the 6,169 Teams that participated in the Challenge including 500 startups.

- **Project Title:** Bring Deep learning and Computer vision capabilities to Shakti Vajra SoC by adding Neural processing engine, MIPI-CSI2 interface and Video processing pipeline
- Responsible for hardware architecture design and FPGA implementation

Merit Cum Means Scholarship

2017 - 2021

Granted tuition-fee waiver during all the undergraduate years